

PD and Signoff for Server Processor

End2End block level execution of 15 blocks for a compute chip

- **Multi-Node Execution:**

Successfully executed (RTL2GDS) **15 blocks** across **3nm and 5nm** technologies
 Netlist2GDS of multiple designs ranging from **1.39M to 5.4M instances** and **176–330 macros** per block, with frequencies up to **1.3GHz**

- **High-Frequency STA Closure:**

Achieved signoff for **high-performance compute blocks** through rigorous setup/hold fixes, **DRV/DRC/shorts resolution**, and **EM violation mitigation**
 Implemented **Viapillar structures** to address critical electromigration risks



1 Lead
7 Engineers

- **Timing & Congestion Optimization:**

Fixed **critical timing violations** and congestion hotspots
 Automated **timing ECO flows** using **Tweaker & DMSA (PTSI)**, running multiple iterations for rapid convergence



1 Year

- **Efficiency & Automation:**

Developed **Make flow scripts** for timing summary reports, accelerating debug
 Resolved **physical verification (PV) issues** using **Calibre**

Results:

- Executed full RTL-to-GDS flow for complex memory blocks with clean DRC/LVS and robust EMIR signoff, meeting all tapeout requirements

Tools: Innovus, Primitime, ICC2, Star RC, Calibre, Tweaker, Conformal

Tech nodes: 3nm, 5nm

