

PD and Signoff for Mobile Processor Client

End2End Low power design(100+ block level implementation) on multiple programs

Executed end-to-end low-power implementation:

UPF & Constraints: Defined power domains (multi-voltage, power gating) and timing constraints

Implementation Flow:

- Power-aware synthesis, floorplanning, and IR-drop-optimized power grid
- Congestion-aware placement, Low-skew CTS, Route optimizations with leakage recovery and ECO-driven ARM Core hardening

Sign-Off: STA (pre/post-layout), LEC, and CLP for power intent validation

Tools: Design Compiler, ICC2, Innovus, StarRC, Primetime SI, Formality, Conformal Low Power, Tweaker

Tech nodes: 3nm, 4nm, 5nm, 7nm TSMC



2 Leads
30+ engineers



4+ Years (On going)

