

# PD & Signoff for Graphics Processor Client

RTL-to-GDS closure for 50+ partitions across 5nm (top die) and 22nm (bottom die) in a 3DIC with TSV integration, multiple power domains, and complex clocking

## Solution:

- End-to-end execution from synthesis to routing with TSV-aware implementation
- Advanced power planning for multi-voltage domains
- Complex clock tree synthesis across dies
- Hierarchical STA closure for all partitions



2 Leads  
25 Engineers



2 Years

## Results:

- Successfully implemented 50+ blocks
- Optimized 3DIC integration with robust TSV handling
- Met aggressive tapeout schedule

**Tools:** Fusion Compiler, Primetime, Calibre, ICV, Redhawk-SC

**Tech nodes:** 5nm & 22nm

