

# DFT for Multi-partition server/client design

Perform high test coverage and robust post-silicon validation for complex designs through structured ATPG methodologies and GLS verification

## Solution:

- **End-to-End ATPG Execution:**

- Performed ATPG DRC analysis & fixes, ensuring compliance with design rules
  - Improved test coverage for Stuck-at, At-speed, and Cell-Aware fault models
  - Generated Intest, Extest, and Alltest patterns with rigorous no-timing & timing validations



1 Lead  
2 Sub-leads  
15 Engineers

- **Seamless Pattern Handoff & Debug:**

- Delivered production-ready patterns for manufacturing test
  - Provided pre- & post-silicon debug support, resolving critical issues for faster bring-up



1+ Years (On going)

- **GLS Validation:**

- Verified pattern integrity through Gate-Level Simulation (GLS) to ensure silicon correlation

## Results:

Successful execution of ATPG/Simulations/ Post Silicon Debug on multiple programs, 48+ partitions

**Tools:** Siemens Tessent Tool, Synopsys VCS & VERDI

