

DFT for Mobile Processor

Performing ATPG, GLS, Scan Insertion & MBIST Simulations on multiple projects

Solution:

ATPG & GLS:

- Full ATPG implementation (Intest/Extest)
- Timing & no-timing pattern validation
- Spyglass DRC checks
- Generated production patterns: Stuck-at • At-speed • IDDQ • Bridging for all



1 Lead
6 Engineers

Scan Insertion & MBIST Simulations:

- Scan Insertion at core & subsystem level
- MBIST Simulation both Non-Repairable and Repairable Memories



2+ Years (On going)

Results:

- Successful execution of ATPG/Simulations on multiple projects, 15+ partitions for each project
- Successful execution of Synth-DFT for multiple subsystems with TPI insertion

Tools: Siemens Tessent Tool, Genus, Xcelium & Synopsys VCS

