

# Chiplet Verification for AI Accelerator Chip

Chiplet that is part of a full-scale AI accelerator chip

## IP Level/Subsystem Level/SoC Level:

- Automation of the VIP integrated testbench environment using python script (UTB - Universal Test Bench)
- Test plans for each IP, Subsystem and SoC
- Creation of reusable testbench for each IP, Subsystem and SoC
- UVM based constraint random verification environment
- Integration of 18 Synopsys VIPs for IP, Subsystem and SoC level verification
- Control and Status Register verification using RAL
- Set-up related to VSO.ai to automate the coverage and regression optimization
- VCD to Verilog and Signal tracker script
- Sign-off through Code and Functional coverage, and Regression pass rate



1 DV Lead  
14 Engineers



14 Months

## Subsystem blocks:

- Compute Unit Subsystem, Scale Out Subsystem Verification

