

CXL-Based Smart Network Controller Verification

- Provides the ability to expand or pool DDR memory, PCIe/CXL storage/memory
Connect to numerous host servers with high-bandwidth and low-latency
- SoC level:
 - Verification of primary external interfaces: DDR4/DDR5, PCIe, CXL
 - Verification of external interfaces: JTAG, I3C, QSPI, UART, GPIO
 - Formal verification for connectivity
 - Gate level simulations (zero delay, min and max corners) and Xprop
 - Power aware verification
 - SoC feature detailed test plan and test plan for each subsystem
 - UVM Based constrained random verification environment
 - Sign-off through functional coverage, regression pass rate
- Subsystem:
 - PCIe (32 lanes), CXL Controller Block, Performance Resource Director, System Level Cache, DDR Memory Block, Security Block
 - SoC with stub-based subsystem verification



2 DV Leads
16 Engineers



24 Months

