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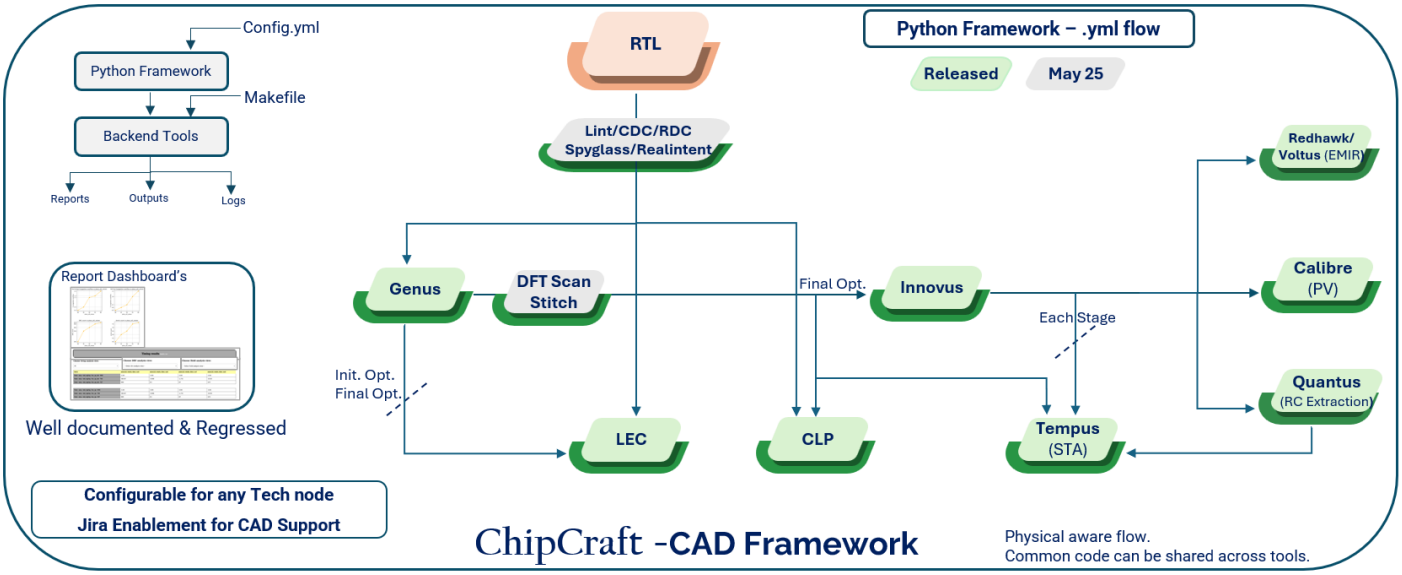
TECHNOLOGIES

ChipCraft

A Comprehensive RTL2GDS CAD Flow for Custom Application



In today's rapidly evolving semiconductor industry, the demand for efficient, scalable, and customizable design flows is higher than ever. To address this need, we have developed **ChipCraft**, a robust RTL2GDS CAD flow that provides a simple, comprehensive, customizable solution for turnkey execution. Built on a Python framework with YML-based configuration and Makefile control, ChipCraft simplifies the design flow and Designers can use our performance-power-area (PPA) recipes to meet their specific design goals in today's demanding semiconductor landscape.

A Unified and Scalable Framework

ChipCraft integrates state-of-the-art EDA tools into a centralized, scalable, and systemized workflow. The framework adheres to the **4S principles**—Simple, Scalable, Stable, and Systematic, making it adaptable to stitch multiple EDA flows that can be used for a wide range of applications, from small IP blocks to full-system SoCs.

Key features include:

- **Genus Synthesis Flow**: Supports advanced PPA techniques such as datapath optimization {Analytical Optimization, Sharing Transformations, Speculation Transformations, Carry-Save Adder Transformations, Timing driven Architecture Selection}, iSpatial flow, clock mapping, Timing optimization {Ungrouping, Retiming, Path grouping}, Area optimization {Multibit inferencing, Boundary optimization} and power optimization. Features like retiming, path grouping, and cell biasing enable designers to achieve optimal timing and area results.

- **Innovus Implementation Flow**: Offers customizable options for placement, clock tree synthesis (CTS), and routing. Over 30+ utilities developed for PPA enhancement/ Quality improvement at each stage of the PD flow; eg: place_fix_congestion, early_clock_flow, post_route_drc_fix, etc.
- **Sign-off Flows**: Employs Logic Equivalence Checking (LEC), Tempus/Primetime for Static Timing Analysis (STA) with MMMC & ECO flow, Conformal Low Power (CLP) for power optimization, Calibre for physical verification, and Voltus & Redhawk for Electromigration and IR Drop (EMIR).
- **Dashboards**: Intuitive GUI tools for metrics comparison, timing analysis, and visualization of synthesis and PnR results, enabling quick decision-making.

Customization and PPA Optimization

ChipCraft is designed for flexibility, allowing users to tailor the flow to specific project requirements.

Key customization features include:

- **Optional Settings**: Users can enable or disable features with ease like useful skew, layer promotion, and congestion fixes based on design needs.
- **Pre- and Post-Hook Scripts**: Custom TCL/Python scripts can be integrated at any stage for ad-hoc testing or optimization.
- **PPA Recipes**: Pre-configured optimization strategies for power, performance, and area, such as multibit cell inference, clock gating, and dynamic power optimization.

Proven and Ready for Deployment

The flow has been rigorously tested on multiple 22nm TSMC designs, ensuring reliability across varied use cases. With plans to expand to lower tech nodes across foundries and with addition of more tools like Fusion Compiler, Spyglass, Redhawk-SC and more in Phase-II, ChipCraft is poised to meet future challenges.

Seamless Jira enablement for CAD support, ensuring efficient tracking, issue resolution, and collaboration across design and verification teams.

Whether for turnkey projects or internal R&D, ChipCraft provides a **ready-to-deploy solution** that reduces setup time, improves productivity, and delivers superior PPA results. By leveraging this framework, customers can accelerate their design cycles while maintaining high quality and performance.

For more details, contact Mirafra team to integrate **ChipCraft** into your next project.