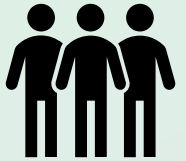
FPGA Prototyping of Multimedia Subsystems in a Tablet chip

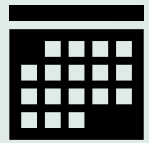
mirafra TECHNOLOGIES

- ASIC Multimedia IP sub-system porting for Xilinx Ultrascale plus FPGA (XCVU19P and XCVU9P)
- Design Integration of FPGA top level including IP subsystem, CPU, Interconnect, DDR4, Clock and Reset Controller.
- Develop bare-metal C/C++ testcases for simulation and FPGA platform bring-up.
- Functional verification of FPGA top level design
- Prepare design constraint
- Synthesis, Place and Route and Timing Closure
- FPGA platform bring-up and use-case validation
- Imagination 3D GPU
- ChipsnMedia Video Encoder/Decoder, 4k Resolution
- Verisilicon Image Signal Processor
- Synopsys MIPI CSI-2, Synopsys MIPI DSI-2
- Digital Blocks Display Controller
- RISC-V CPU
- Arteris NoC

Tools: Xilinx Vivado, Synopsys VCS, GNU C Compiler



1 Technical Project Lead
4 Engineers



Ongoing

ODC with ownership of deliverables