Emulation Of Fibre Channel Chip



Prototyping/Emulation:

- The ASIC consisting of around 6 million ASIC gates is emulated in largest available Xilinx V7- 2000T FPGA.
- The board from Hitech Global "HTG-V7-PCIE-2000" has an additional SFP+ daughter card to communicate with Ethernet
- Convert ASIC design to FPGA compatible.
- · Reset scheme for the emulation design.
- Clock scheme/ratio for the emulation design.
- Create memory wrappers and FIFOs for the emulation design.
- Implement the design using latest Xilinx Vivado Tool.
- Bit-stream Generation with no Timing Violation.
- Debug

Synplify, Vivado, Verilog, C, Perl





6 months



T&M with ownership of deliverables