Memory layout 5nm

Customer : The customer is a tier-1 company.

Project : Memory layout development on 5nm.

Mirafra's Responsibility :

- Develop all sub blocks like row and column decoder, control, array for memory.
- Memory level integration of all sub block.
- Supporting different functionality like column mux, Redundancy , Power gating.
- Matching for Sensor amplifier.
- LEF generation. EM/IR cleaning. Design closure DRC , LVS, ERC, EM/IR, DFT, Density

Tools used : Custom Compiler (Synopsys), Calibre (Mentor)

Engagement Model : A team of 3 people for 8 months year onsite based on T&M model.