Memory Layout 3nm

Customer : The customer is a tier-1 company.

Project : Compiler development in TSMC 3nm Technology

Responsibilities:

- Layout development from scratch from leaf cells to instances.
- Full instances different combinations DRC/LVS cleaning , design implementation.
- Full compiler list DRC/LVS cleaning
- Area decision and development of new feature with row redundancy block from scratch with instance Level DRC/LVS cleaning
- Lef related activities.
- Development of IO for row redundancy for different mux1 combinations (like single/multi bank)

Tools Used : Cadence Virtuoso , calibre for DRC/LVS.

Engagement Model : 4 persons for 6 months on T & M model