## Memory Design - 3nm

<u>Customer</u>: The customer is a tier-1 company.

**<u>Project</u>**: Memory Design on 3nm

## **Mirafra's Responsibility**:

- Global control design from scratch for Duel rail power implementation
- Driver power management, Standby operation support and ISO control for power saving.
- Analyzing the peak current and current distribution across the whole memory macro.
- Monte-Carlo simulations, ,frontend/backend view generation and QA.
- Signoff with the characterization across PVT corners.

<u>Tools used</u>: Virtuoso (Cadence), Finesim(Synopsys), Solido (Mentor Graphics)