Memory Design -7nm

Customer : The customer is a tier-1 company.

Project : SRAM mixed VT memory design aimed at optimizing leakage and improved timing

Mirafra's Responsibility :

- Primary objective to enhance data access speed and read/write operations and reduce power consumption(reduced leakage).
- Research on existing design wherein to identify the best elements to incorporate into the mixed-model.
- Conducted leakage and timing analysis utilizing mixed model design
- Simulation for evaluating the Timing and Leakage
- Based on the timing and leakage data, the base design is identified, margin is run on the selected design.

Tools used : Virtuoso (Cadence), Finesim(Synopsys), Solido (Mentor Graphics)