Memory Design - 7nm

Customer : The customer is a tier-1 company.

Project : Memory Design development on 7ff.

Mirafra's Responsibility :

- Design and feasibility for initial schematic development which includes bit-cell read stability and writability.
- Analyzing functional margins at different PVTs to check for robustness of the design.
- Montecarlo analysis on few sensitive circuits.
- QA for all the views generated.
- Sign off with Characterization.

•**Tools used** : Virtuoso (Cadence), Finesim(Synopsys), Solido (Mentor Graphics)