Delta-Sigma modulator IP layout in 16nm

Customer : The customer is a tier-1 company.

Project : The Delta-Sigma modulator IP with an innovative design for power efficiency was designed in state of art 16nm.

Mirafra's Responsibility : Mirafra was involved in completion of Delta-Sigma modulator IP layout.

- Floorplan of complete Delta-Sigma modulator IP taking care of signal flow and layout of sub-blocks.
- Power routing and signal routing of entire Delta-Sigma modulator IP.
- Context dependency layout to take care of coupling, matchings, STI, LOD etc.
- Dummy fill, density checks etc complete delivery of Delta-Sigma modulator IP.

Challenges: Compacting the floorplan, symmetry, routing of capacitors. Context dependent challenges in sub blocks like symmetry.

Tools used : Virtuoso (Cadence), Calibre (Siemens)

Engagement Model : 2 members for 3 months on T & M model