Temperature to Digital (TDC) layout in 5nm

Customer : The customer is a tier-1 company.

Project : The TDC IP was designed in state of art 5nm process node.

Mirafra's Responsibility : Mirafra was involved in completion of TDC IP layout.

- Floorplan of complete TDC taking care of signal flow and layout of sub-blocks.
- Power routing and signal routing of entire TDC.
- Context dependency layout to take care of coupling, matchings, STI, LOD etc.
- Dummy fill, density checks etc complete delivery of TDC.

Challenges: Symmetric floor planning. Context dependent challenges in sub blocks

Tools used : Virtuoso (Cadence), Calibre (Siemens)

Engagement Model : 3 members for 3 months on T & M model