Rx IP (5Ghz) layout in 14nm

Customer : The customer is a tier-1 company.

Project : The Receiver IP was designed in state of art 14nm process node.

Mirafra's Responsibility : Mirafra was involved in completion of Receiver IP layout.

- Floorplan of complete Receiver IP taking care of High frequency signal routing, coupling, RC etc.
- Power routing and signal routing of entire Receiver IP.
- Context dependency layout to take care of matchings, STI, LOD etc.
- Dummy fill, density checks, colouring etc complete delivery of Receiver IP.

Challenges: High frequency routing, Power planning, Creating ESD protection structures as the inputs are connected to I/O to bumps.

Tools used : Virtuoso (Cadence), Calibre (Siemens)

Engagement Model : A team of 3 members on T & M model for 6 months