LPDDR3/4 Rx (22/14nm) Design

LPDDR34 RECEIVER				
Parameter	Value			Unit
	min	typ	max	
IO Supply Voltage	1	1.1	1.2	V
Core Supply Voltage	0.72	0.8	0.88	V
Operating temperature range	-40		125	C
Common mode range LPDDR4	10%		42%	% IO Supply
Common mode range LPDDR3	49%		80%	% IO Supply
Input slew rate	1	4	7	V/ns
Input swing	0.08		Vddio/2.5	V
Cross point variation	-0.25*swing		+0.25*swing	V
Input capacitance			0.15	pF
Frequency	400	1067	2133	MHz
Duty Cycle	47	50	53	%
IO Average current			1.75	mA
Core average current			2.8	mA

- Project: LPDDR34
  - Technology: 14nm/22nm
- Work Done:
  - Architecture selection
  - Circuit design and Schematic implementation
  - Simulation across PTV corners
  - Protocol compliance and timing analysis
  - High level power analysis
  - SOA(Safe Operating Area) analysis
  - Monte Carlo Analysis
  - Leakage Analysis
  - Post layout simulation and Starrc netlist
  - Signal integrity analysis, EMIR
  - PDK Evaluation
- Team size:
  - Lead: 1
  - Circuit Designer: 2
  - Layout Engineer: 2
- Project Duration: 6 months