Tx (7nm) Design:

Transmitter(@6.4Gbps)				
Parameter	Value			Unit
	min	typ	max	
Core Supply Voltage	800	850	900	mV
IO Supply Voltage	400	450	500	mV
Operating temperature range	-40	70	125	C
EMIB Channel length	-	-	2	mm2
Incoming clock slew rate	15	35	40	pS
Incoming Differential clock overlap	-	-	5	pS
Incoming data slew rate	-	-	55	pS
Max Bandwidth/mm2			1.5	Tbps
Driver Pull up/ Pull dn Impedance	18.5	20	25	Ohms
Impedance Mismatch	-	-	0.5	Ohms
Delay Mismatch between pull up/ Pull dn	-	-	4.5	pS
Pad DCD at Rx Input	-10	-	10	pS
Lane to lane Skew	-16		16	pS
Tx Pad cap	-	-	300	fF
Data Rx Pad cap	-	-	300	fF
Clock Rx Pad cap	-	-	300	fF
ESD Rating: Charge Device Model	-	0.5	-	A
Frequency	-	3.2	-	GHz
Idle Power	-	-	30	mW
Maximum Data rate	-	-	6	Gbps
Reliability Verification	-	-	4	Years

- Project: Transmitter-1
  - Technology: 7nm
- Work Done:
  - Architecture selection
  - Area analysis with multiple form factors (aspect ratio)
  - High level power analysis
  - Support for System level integration, package, bump ball map
  - Circuit design and Schematic implementation
  - High Level Floorplan implementation
  - Detailed Layout analysis and implementation
  - Complete physical verification, antenna
  - Signal integrity analysis, EMIR, GB, timing – for critical paths
  - Signoff checks - metal fill, density checks
  - Testability / DPPM checks
  - Final Tapeout checks and signoff
- Team size:
  - Lead: 1
  - Circuit Designer: 4
  - Layout Engineer: 4
- Project Duration: 1Year 6 months