Low Power SAR ADC Design/Layout (45nm)

Customer : The customer is a Top tier Semiconductor Company.

Project : The low power SAR ADC was designed in 45nm process. It was a 12bit ADC.

Mirafra's Responsibility : Mirafra was involved for completion of Design & Layout with following specifications.

- 12-Bit Resolution with NMC
- Unipolar Input Range: 0 V to AVDD
- AVDD: 1.65 V to 3.6 V
- Integrated Offset Calibration
- 234 µW at 1 MSPS with 1.8-V AVDD

Tools used : Cadence Schematic suite, Spectre, Cadence Virtuoso & Calibre.
Engagement Model : A team of 2 Designer and 2 layout designer for 3 months onsite based on T&M.