SerDes – Layout (7nm)

Customer : The customer is a tier-1 company.

Project : The Serdes was designed in state of art 7nm process.

Mirafra's Responsibility : Mirafra was involved in completion of TX and RX layout.

- Floorplan of complete TX delivery.
- Contribution to RX layout design.
- Innovative buffer design for output of clock channels going to Final driver.
- Context dependency layout to take care of coupling, matchings EM etc.
- ESD related checks for Clamp diodes.

Tools used : Virtuoso (Cadence), Caliber (Mentor)

Engagement Model : A team of 5 people for 1+ year onsite based on T&M model.