LDO & BGR (45nm) Design:

LDO SPECIFICATION

Parameter	Value			Unit
	min	typ	max	
Input voltage	2.1		3.6	V
Operating temperature range	-40	27	125	C
Output Voltage		1.8		V
Dropout Voltage		0.3		V
Load current	0.1		3.0	mA
Quiescent Current	15		200	uA
Load Regulation		0.6		mV/mA
Line Regulation		0.24		mV/V
Output capacitance(off chip)		1.0		uF
ESR	0		300	Ohm
PSRR	-70			dB @ 1Khz
Technology/Fab		40 nm/TSMC		

BGR SPECIFICATION

Parameter	Value			Unit
	min	typ	max	
Supply voltage	1.72	1.8	1.98	V
Operating temperature range	-40	27	100	C
Reference voltage	1.2	1.22	1.25	V
Current consumption		46	66	uA
Leakage Current			10	nA
Vref deviation			1.5	%
TC			9	ppm/C
PSRR	-60			dB @ 100Khz
Technology/Fab		40,65nm/TSMC		

- Project: LDO-1
  - Technology: 40nm
- Work Done:
  - Architecture selection
  - Area analysis with multiple form factors (aspect ratio)
  - High level power analysis
  - Support for System level integration, package, bump ball map
  - Circuit design and Schematic implementation
  - High Level Floorplan implementation
  - Detailed Layout analysis and implementation
  - Complete physical verification, antenna
  - Signal integrity analysis, EMIR, GB, timing – for critical paths
  - Signoff checks - metal fill, density checks
  - Testability / DPPM checks
  - Final Tapeout checks and signoff
- Team size:
  - Lead: 1
  - Circuit Designer: 2
  - Layout Engineer: 2
- Project Duration: 4.5 months