GPU, Camera & Modem Teams RTL2GDS2 (10nm)

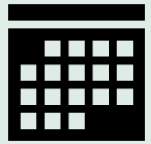
mirafra TECHNOLOGIES

Mirafra team was involved in a Front to Backend Multi-hierarchy Lead Led project design

- **Specify Design Constraints sdc & generate synthesized netlist**
- **Own the pre-layout and post-PnR STA of the design**
- **Own portions of LEC & CLP checks & UPF ownership of the design**
- **Ensure Full Chip time budgeting and Partitioning of the blocks**
- **Implement the Low Power aware PnR as per the specified Design Constraints**
- **Close hierarchical Timing violations in multiple iterations**

Tools: Design Compiler, RTL Compiler, Formality, Conformal Low Power, ICC2, Innovus, Primetime

10 Engineers



12 months

Onsite based on T&M