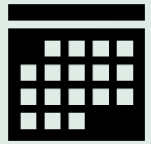
RTL Design And Verification of AXI BIU IP

mirafra TECHNOLOGIES

- RTL design of AXI BIU IP from scratch and contributions to the specification document , microarchitecture & design document
- Implementing Front End Design TFMs like SG-Lint, SG-CDC, VCLP, Synopsys DC, Caliber, Fishtail
  - Ownership of Lint, CDC and Synthesis
  - RTL Bug Fixes
  - RTL releases for 0.3, 0.5, 0.8 and 1.0 milestones
- Implementing Verification Environment in UVM
  - Ownership of Implementing the Verification Environment starting from verification plan to Implementation in UVM
  - Verification releases with various features for 0.5,0.8 and 1.0 milestones

1 Project Manager
5 Engineers



Ongoing since 10 months

T&M with ownership of deliverables