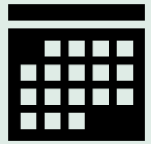
RTL Design And Integration Of Arteris NoC

mirafra TECHNOLOGIES

- NIU interface details (Protocol info, Clock & Power domains) and connectivity info + Memory mapping of Master NIU's incoming transaction
- (Read/Write) to Target NIU
- Defining the Interconnect Data/Service path Topology : placement of De-mux , Buffer (Async FIFO, Sync FIFO/Rate Adapter, Mux)
- For FPGA/Silicon Debug related logic addition i.e. various type of Probes and Event collector.
- Lower Power RTL: Clock gating controllers for micro/macro sleep scenario.
- NoC sub-system integration with Client IP/3rd Party IP : SRAM, Client IP (SRAM redundancy decoder , Analog Power-Mux, CPR Sensor), Client common IP (Flop-Memories, CDC Synchronizers ,Clock gates) and 3rd Party IP (Arm Coresight components) etc.
- Design Power Intent and check sanity with Cadence Conformal Low Power tool.
- RTL sanity and CDC : Spyglass Lint and CDC checks.
- Review of various waveforms : Core DV / SoC DV (Functional and Power-aware Functional verification) Simulations. Also, Performance-team simulations

1 Design Engineer
Client SoC Design Team



Ongoing

Individual Contribution at client site