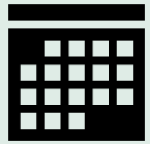
RTL Design - Neural Engine interface and control for Automotive SoC

mirafra TECHNOLOGIES

- **Instruction & Data DMA Blocks Micro-Architecture & Implementation**
- **Programmability for multiple types of DMA, including LinkedList's**
- **AXI Interface to system NoC**
- **Hardware-Handshake-based flow control**
- **Instruction Sequencer Integration**
- **Scalable and versatile data set fetching**
- **System Verilog test bench for sanity check**

AXI, APB, AHB, Smart DV DMA IP, Synopsys DMA Controller

1 Lead
1 Program Manager
3 Engineers



6 months

ODC with ownership of deliverables