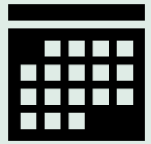
RTL Design – MPC PMbus IP

mirafra TECHNOLOGIES

- Ownership of Digital Multiphase Controller PMbus module
- Project Planning including definition of Tasks, Milestones and RTL Releases
- Complete ownership of Micro-architecture definition to RTL sign-off
  - SMBus and AVS bus modules development with path flush
  - Register map Generation and Integration
  - Lint, CDC, Synthesis and Timing report analysis/design update
- Working closely with the Verification team
  - Test Plans
  - Sign-off with zero bugs
- Tools : Questsim, xcelium, spyglass & Genus

1 Design lead
2 Engineers



7 months

ODC with ownership of deliverables