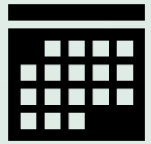
# Physical Design For Hard Macros, Full-Chip SOCs (7nm & below)

mirafra TECHNOLOGIES

- **Floorplan completion optimized on Area based on Full chip specifications**
- **Build clock-tree (different techniques), with special consideration on power and skew**
- **Placement & routing for high frequency, multi-clock & power domain designs**
- **Static Timing Closure and ECOs across multiple corners**
- **Closing DRCs including Dual patterning on low process nodes (7nm & below)**
- **Automation of the Common operations in PnR execution & reporting**

**Tools: ICC2, Innovus, Primetime, Tempus, Calibre**

**8 Engineers**



**24 months +**

**T&M with ownership of deliverables**