Graphics Multi-Die design Netlist2GDS (5nm & 22nm)

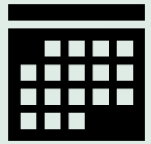
mirafra TECHNOLOGIES

Mirafra team is involved in PD & STA of both Dies. Owning the complete STA execution of Base Die under lead-led model

- **Running & Driving Fullchip Timing Constraints & Validation**
- **Floorplan to Route-Opt, LV, Power and Timing Clean up**
- **Scripting to fix timing, Routing, Custom Clock tree and LV issues**
- **Timing for multi-die paths across all scenarios**
- **Complete ownership for Scan mode Timing**

Tools: Fusion Compiler, Primetime

30 Engineers



12 months

Onsite project