Bench Characterization



- Characterized different IP/Interfaces across PVT
- Own Bench Test Plan, Bring up, Debug and PVT Analysis
- Automation using LabVIEW and Python
- Power Management
 - Buck, Boost, LDO, Integrated regulators, VREF
- Clock System Oscillators, PLL
- Data Converters DAC, ADC
- SERDES, GPIO
- PHY DDR, MIPY D-PHY and C-PHY, USB3, USB2





To be Updated



T&M with ownership of deliverables