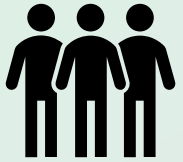
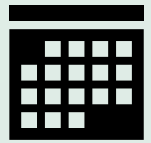
CPU SS Validation – Slide 1/2

mirafra TECHNOLOGIES

- CPU Core Validation
  - Code execution and data access
    - From Different Memories
    - Different Exception Levels
    - Secure and Non-Secure Modes
    - Different Clock Sources
  - Multi-Core Features
  - Power down mode entry, exit and power measurement
  - Exception Handling
  - Timer Operation
  - Security Aspects
  - Debug Features
  - Different Frequency-Voltage Plans
  - Vmin and Fmax Analysis across PVT
- Interrupt Controller Validation
  - Interrupt Processing in Secure and Non-Secure Mode
  - Affinity routing
  - Supported Interrupts



2 Engineers



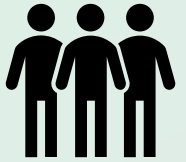
6 months

T&M with ownership of deliverables

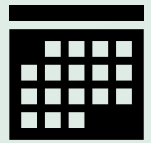
CPU SS Validation – Slide 2/2

mirafra TECHNOLOGIES

- Cache Memory Validation
  - Cacheable and Non-cacheable Access
  - Invalidate and Clean
  - Supported configurations
  - Supported Cache line sizes
  - Cache Policies Supported
  - Latency and Performance Measurement
  - Coherency validation
  - Operation as SRAM
- MMU Validation
  - Address Translation - Level 1 and 2
  - Supported Page Table Formats and Page Sizes
  - Memory Attributes - Access Permissions, Memory Type, Cache policies
  - Fault scenarios
  - Secure/Non-Secure Access
  - TLB invalidate and Flush



2 Engineers



6 months

T&M with ownership of deliverables