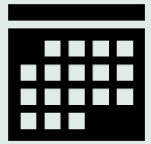
PD & DFT-ATPG for a Multi-partition cutting edge graphics Design (10nm)

mirafra TECHNOLOGIES

- **Involved right from generating DFT patterns, simulating and ensuring that the Scan functionality was implemented and fully functional on Silicon**
- **Lead led model for PD & DFT for ~100 partitions of a full SoC design**
- **Deep understanding of Multi-Clock design, Hips and EDT functionality**
- **Multi-Power domain, high frequency timing closure for many sub-systems**
- **Generated Stuck-At & At-speed patterns for all partitions**
- **Interfaced with RTL, PnR and ATE teams for different Logic and Scan functionality**
- **Generated post-silicon patterns and supported Power On and Silicon Bring up activities**

Tools: Mentor Tessent, Synopsys Tetramax

1 Lead
10 Engineers



24 months +

T&M with ownership of deliverables