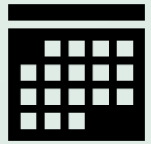
Networking ASIC Verification

mirafra TECHNOLOGIES

- **Partial ownership of full chip verification and complete ownership of several blocks within a multimillion gate Networking chip using Constraint random verification methodology**
- **Architected many parts of the test bench from scratch**
- **Develop comprehensive feature-set based test plan and functional coverage plan**
- **Execute functional verification and run regressions.**
- **Bug reviews with design team and closure with detailed documentation**
- **Coverage (code & functional) closure**
- **Filled checklist items for TO**

Verification Language & Methodology : SV, VMM

10 DV Engineers



18 months

T&M, Execution at client location