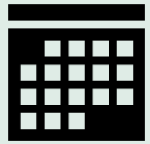
Design & Verification of MPC PMBus and other IPs

mirafra TECHNOLOGIES

- **RTL Design & Verification ownership of Digital Multiphase Controller PMBus module**
- **Complete ownership of Project Planning, micro-architecture definition and RTL Development of PMBus IP**
- **SMBus and AVS bus modules development with path flush**
- **Lint, CDC, Synthesis and Timing report analysis/design update**
- **Verification of PMBus using UVM at block level and hybrid environment (C plus UVM) at SoC level from scratch**
- **Synthesizable transactors development using SV and UVM with the different views : Simulation, Emulation and FPGA**
- **Complete ownership of Design verification from Verification specification definition to the Signoff**

1 Design Lead
1 DV Lead
1 Program Manager
4 Engineers



10 months

ODC with ownership of deliverables