MBIST support for 14nm, 22nm & 28nm IPs

mirafra TECHNOLOGIES

- Team worked on MBIST Insertion at the RTL stage. Inserted Scan Insertion at Synthesis stage as well
- Worked on MBIST Controllers for multiple Memory blocks
- Generate MBIST Patterns along with standard ATPG simulations
- Run Timing and No-timing simulations
- Work with RTL, Synthesis and STA team to improve the Scan functionality
- Post-Silicon pattern support including Pattern Generation and Diagnosis of tester data

Tools: Mentor Tessent

1 Lead Engineer
4 Engineers

60 months

Onsite based on T&M