Scan Insertion & Full Chip Integration of Scan Logic

mirafra TECHNOLOGIES

- Insertion of OCC and the supporting clocks for DFT
- Fixing of the DRCs at Scan Insertion stage
- Fixing of the faults to improve the coverage
- Worked on timing files (min/max.sdc) and analyze the setup or hold violations in Gate Level simulations
- Path Delay patterns generation & transition pattern analysis
- Debugged multi-Clock challenges in Scan insertion & Simulation

Tools: DC, Genus, Mentor Tessent

5 Engineers

24 months +

T&M