DFT, MBIST & Post Silicon Support for Full Chip SoC

mirafra TECHNOLOGIES

Mirafra team was involved in a ATPG, MBIST and Post Silicon Support for a Full Chip SoC design

- Pin planning and MBIST Integration in the Full chip SoC
- Power domains & requirements for different Memory Ips for which we generated Patterns separately
- Worked on TDR programming & JDR programming
- Worked on ITPP (Test procedure files) for cut-point insertion & debug at multiple hierarchies
- Debugged Post-Silicon Diag logs, debugging them systematically between Simulation and ITPP runs and tracing the paths to fix the reasons of Silicon failure

Tools used : Mentor Tessent, Synopsys Tetramax

10 Engineers

12 months

Onsite based on T&M