VERIFICATION USING SV, UVM OF FPGAS FOR NETWORK ROUTERS AND LINE CARDS

The Customer:
Customer is the worldwide leader in networking and switching, router products.

The Application:
These FPGAs perform functions like network aggregation, line card control, router chassis control and act as offload engine for additional networking protocols like BFD. The designs were implemented using Xilinx Zync or Spartan 6 family devices.

Mirafra's Responsibility:

- Complete ownership of functional verification of the FPGA design using UVM.
- Integration of verification environment based on the supported features.
- Development of parts of the test bench from scratch.
- Porting existing legacy VMM environment and BFMs to UVM.
- Development of UVM based infrastructure for easy reuse between future projects.
- Regression of test cases and analysis of the results.
- Provide support during FPGA validation in the lab.

Engagement Model:
A team of three engineers for twelve months onsite based