PHYSICAL IMPLEMENTATION OF OCTA/HEXA/QUAD CPU/GPU CORE FOR MOBILE CHIP

The Customer:
A world leader of wireless and CDMA technologies

The Application:
Targeting the true 64 bit architecture for advanced cell phone chips with different processors for different market segments

Design Specifics:
Speed up to 1.7GHz, with 20nm technology, blocks upto ~ 8mm2 with 180-200 memories/macros & 7-8 power domains

Design Challenges:

- Power domain aware CPF/UPF enabled floorplan/placement
- Complex iterations for CTS/Routing for design closure with minimal number of metal layers
- Excessive non default routing for extremely aggressive yield targets

Mirafra's responsibility:

- Complete ownership of netlist-to-GDSII which comprised STA timing closure, Reliability & Physical verification sign-off
- Post Base freeze, precise calculation and implementation of functional eco (or any other ECOs) with least disturbance in database and handling the disturbance manually
- Active contribution on all issues in flow & design and providing simple and portable solutions with least effort for user
- Engagement in verification of LEC and CLP for early identification any issues after every changes made in design

Tools used:
Synopsys IC-compiler, PT-SI, Caliber, Cadence LEC and Cadence CLP

Engagement Model:

TNM, one person handling upto 4 blocks for the closure with a tape-out cycle of 3-4 months