FULL CHIP AND MODULE LEVEL VERIFICATION OF A MULTI-MILLION-GATE ASIC

The Customer:
Customer is the worldwide leader in networking and switching, router products.

The Application:
The application is a 34 million gate count ASIC whose primary functions include virtual output queuing, fabric high availability and local and central arbitration support. It finds its use in ultra-high speed line card range of products. It is a complex chip comprising 15 modules, multiple clock domains and many IP's. The ASIC communicates with other IP's and with the CPU through high-speed interfaces (up to 15 Gbps).

Mirafra's Responsibility:

- Ownership of functional verification of several modules within the ASIC.
- Full chip verification of the ASIC using System Verilog and VMM methodology.
- Architecting portions of the test bench from scratch.
- Integration of various IP's and functional verification of the integrated system.

The Challenges:

- Aggressive timelines.
- Complexity of the ASIC, several IP's, multiple clock domains, 15 modules.
- Working on multiple tasks at the same time, always being ready for a new challenge to come our way at short notice.
- Dealing with inadequate or in some cases inaccurate specification documents.

The Solutions:

- Meetings were setup in the first week with the client lead engineers to understand various aspects of the ASIC, including its architecture, timelines etc.
- In order to expedite the process of specification understanding, Mirafra team members split the document between them such that each member became an expert on a certain section and shared this knowledge with the rest of the team. Organized follow-up meeting with client to plug any holes in spec understanding.
- Proactive approach was demonstrated by Mirafra engineers who would follow up with client team diligently to resolve outstanding issues. Meetings were used to escalate issues that were

not being resolved in a reasonable amount of time. If a deadline was not practically achievable, a heads up was given to the client to help them plan accordingly. This was appreciated by client.

- Effort was made to help each other out by reassigning work between team members depending on how much each team member was loaded. Client team was kept in the loop on such reallocation of work. This team spirit was instrumental in us achieving our combined goals.
- Program manager from Mirafra sought feedback from the client periodically to ensure that team was on the right track and to course-correct if necessary.

Technical Tasks Completed:

- Full chip verification of the ASIC using System Verilog and VMM methodology was done.
- Architected many portions of the test bench from scratch.
- Integration of various IP's and functional verification of the integrated system was completed.
- Completely owned functional verification of several modules within the ASIC.
- Developed comprehensive test plans and functional coverage plans.
- Created constrained random verification environment and generated several test cases and scenarios by this methodology.