VERIFICATION OF LPDDR3 CONTROLLERS USING SV & UVM

The Customer:
Customer is a world leader in smartphone and tablet SoCs.

The Application:
LPDDR3 controller is used in all customer SoCs to support different memory requirements. The controllers are implemented as per JEDEC LPDDR3 standard.

Mirafra's Responsibility:

- Development of complete verification environment for LPDDR3 controller in System Verilog using UVM methodology.
- Definition, architecting and coding of UVM based test bench so that it is reusable across multiple LPDDR controller revisions.
- Coding and debugging of test cases.
- Development of assertions for interface level protocol checks.
- Driving verification to closure using regression, functional coverage and code coverage metrics.

The Challenges:

- Understanding design specification, and coming up with features and scenarios inside the first two weeks.
- Developing complete verification environment from scratch and coding sanity tests in short span of two months.
- Coding, debugging and regression closure of 150+ tests in four months span.

The Solutions:

- Regular discussions were held among team member to ensure highest quality of verification and to keep tab of project progress.
- Regular meetings were held to analyze issues faced by team members.
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Summary & Achievements:

- Team of two highly competent engineers from Mirafra has owned complete verification of LPDDR3 controller, with verification effort starting from scratch.
- Helped client close the verification by regression analysis and coverage analysis.