VERIFICATION OF A COMPLEX SOC WITH HIGH-SPEED INTERFACES USING SV, UVM

The Customer:
Customer is the worldwide leader in networking and switching, router products.

The Application:
Highly integrated System-on-Chip built on IBM cu45 technology with about 50 million gates and 350 million bits of memories. ASIC supports CE front panel pots, 1Gpbs SGMII dedicated for CPU connectivity and Gen 2.0 PCIe (5 Gbps) Interface for general CPU access. ASIC can be configured to support 2x40GE or 1x100GE and can support 8x2G, 8x4G, 8x8G, 4x16G FC or 8x16G Fiber channel (FC). It provides forwarding functionality for both Layer 2 bridging and Layer 3 routing, supports various L2 and L3 tunnel protocols and crossbar interface/arbitration.

Mirafra's Responsibility:

- Functional Verification of multiple modules within the SoC.
- Full chip verification using System Verilog and UVM methodology.
- Development of test cases and various verification components like monitor, driver etc. for various chip level features which includes Layer2 (bridging) and Layer3 (Routing) forwarding, quality of service for various packet flows and flow control functionality.
- Integration of Gen 2.0 (5 Gbps) PCI Express interface at chip level and verification of the same at parallel and serial interfaces of the chip.
- Verification of all chip level registers functionality using UVM Register Abstract Layer (RAL).
- Analysis of regression results for various chip level test suites at regular intervals.
- Creation of detailed documentation for the environment, test cases, coverage points and bugs.
- Analysis of code coverage results and sign off.

The Challenges:

- Ramping up on TB environment and understanding of complex specification within a short time.
- Aggressive timelines.
- Development of multiple module level verification environments from scratch.
- Verifying timing related cycle specific functionality with automated checking mechanism.

Summary and Achievements:

- Mirafra's team of three engineers worked for 15 months onsite based on T&M (Time & Material) model in collaboration with the client team to successfully tape-out this very complex ASIC.
- Drove the verification to closure by meeting desired sign-off metrics.
- The client team appreciated the efforts of Mirafra engineers for the work.