

TOUCH SCREEN APPLICATION CHIP TAPEOUT

The Customer:

A leader in capacitive touch sensing solutions, touchscreen solutions, powered by Programmable-System-on-Chip technology

Description of the Chip:

This was a mixed signal ultra low power chip for touch screen application. The chip had a microcontroller and programmable logic for communication applications. The analog portion of the chip had several transmit and receive channels, SAR ADC, DAC and on-chip power regulators.

Challenges:

- Low power implementation for several sleep modes needed voltage islands for 'Always ON' and 'Switchable' domains.
- Level shifters and Isolation cells were needed for signals crossing power domains.
- The complexity of the floorplan increased due to the presence of analog blocks with requirements. Getting the information from custom layout into PnR tools was needed.
- For switchable blocks 'State Retention' logic placement and power planning and 'Always-ON' synthesis were required
- ECOs due to functional bugs and power domain related bugs came till the last moment
- Dynamic IR drop was an issue due to the high switching clock buffers

Solution:

IC Compiler was used to floorplan the design into four main voltage areas that needed different power supplies. For two of the blocks that contained 'Always-ON' and 'State Retention' logic secondary power supplies were provided according to the placement of cells. Innovative methodology was designed to bring the Analog routing information from custom layout to the PnR tool. This made efficient utilization of the routing resources and die size was reduced. Scripts were developed to overcome the Dynamic IR drop problem by opportunistic rail sizing.

Outcome:

The chip was successfully taped out within 5 weeks of receiving the final synthesized netlist. It met all the requirements of Low Power implementation.