MIXED SIGNAL VERIFICATION OF A CMOS PHOTONICS BASED HIGH-SPEED ASIC USING SV, UVM

The Customer:
Customer is the worldwide leader in networking and switching, router products.

The Application:
The product is CMOS photonics technology based Layer 1 High Speed Transceiver ASIC. It supports 100G, 4x10G, 2x20G modes with QPSK, FEC and PAM supports for single and multi-mode fibers.

Mirafra's Responsibility:

- Complete ownership of all verification activity on this ASIC.
- Complete architecture and methodology implementation.
- Full chip and Block level verification using System Verilog and UVM.
- Mixed signal verification using AMS based models.
- Integration of new features in the test environment.
- Definition of the complete test suite and coverage.

The Challenges:

- Ramping up on new technology and defining new System Verilog environment based on UVM methodology in short time.
- Understanding of AMS models and mixed signal architecture.
- Development of complete System Verilog based test bench infrastructure from scratch.
- Aggressive timelines.

The Solutions:

- Several meetings were setup in the first week with the client project manager and team to understand various aspects of the project, including architecture, design flow and timelines.
- Meetings were also setup with design engineers to understand block level architecture and critical functionalities to focus during verification.
- As the earlier verification environments were in Verilog, new architecture based on System Verilog and UVM was suggested and several meetings and reviews were conducted to finalize it.

- An automated way to port Verilog tests to newly developed System Verilog methodology to enhance productivity was suggested.
- Mirafra engineers became proficient at Verilog-AMS to understand AMS model behavior in order to enhance debug efforts.
- Program manager from Mirafra would seek feedback from the client periodically to ensure that things were on the right track and to course-correct if necessary.

Technical Tasks Completed:

- Functional Verification at block and full chip level using SV, UVM.
- Developed complete System Verilog based test bench infrastructure.
- Developed and verified high speed and low speed components.
- Developed and verification mixed signal modules using AMS based models.
- Successfully integrated new features in test bench.
- Developed complete test suite.
- Ran regressions and analyzed regression results at regular intervals and worked with designers on closure.
- Automated the regression process.
- Analyzed code coverage results before sign off.
- Created detailed documentation for the environment, test cases and coverage.