GSM/3G ASIC IMPLEMENTATION

The Customer:
Customer is a major mobile maker

The Application:
Physical Implementation of a core module and the full-chip of an advanced ASIC (on 45nm) for GSM/3G mobile application. The full chip had multiple modes of operation and multiple domains of switched power supply.

Mirafra's responsibility

- Complete ownership of Synthesis, LEC, DFT, STA/constraints management, CTS & P&R
- Closely worked with the RTL designers to fine-tune RTL/constraints for the best performance

Tools used:
DC, PT/PTSI, DFT Compiler, Formality (Synopsys), Talus (Magma), Spyglass (Atrenta)

Engagement Model:
A team of 3 people for 4 months onsite based on T&M (Time & Material).