EMULATION OF PI SYSTEM FOR FIBRE CHANNEL CHIP ON HTG-V7-PCIE-2000 BOARD WITH V7-2000T FPGA

The Customer:
Customer is the worldwide leader in networking and switching, router products.

The Application:
The ASIC consisting of around 6 million ASIC gates is emulated in largest available Xilinx V7-2000T FPGA. The board from Hitech Global "HTG-V7-PCIE-2000" has an additional SFP+ daughter card to communicate with Ethernet.

Mirafra's Responsibility:

- Convert ASIC design to FPGA compatible.
- Reset scheme for the emulation design.
- Clock scheme/ratio for the emulation design.
- Create memory wrappers and FIFOs for the emulation design.
- Implement the design using latest Xilinx Vivado Tool.
- Bit-stream Generation with no Timing Violation.
- Co-ordinate with Xilinx Support Team for Tool issues.
- Test Data path and Control path.
- Generate Chipscope probes for debugging.

Engagement Model:
A two member team consisting of engineers who were experts in Xilinx Tools and FPGA's working onsite based on T&M (Time & Material).